

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 5.2 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

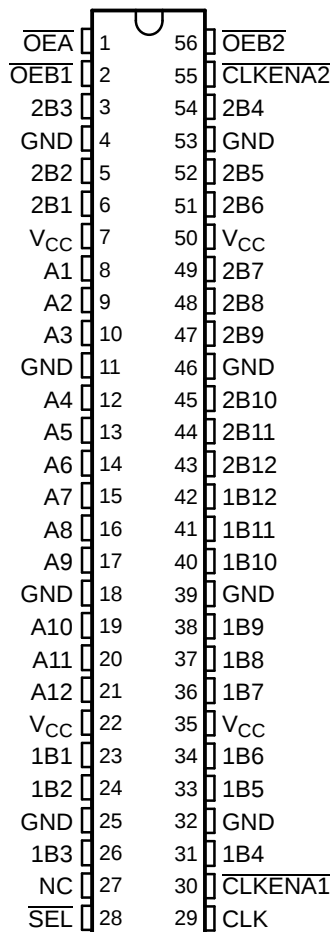
DESCRIPTION/ORDERING INFORMATION

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCHR16269A is used in applications in which two ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input, when the appropriate clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{SEL}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB1}$, and $\overline{OEB2}$).

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ALVCHR16269AL	ALVCHR16269A
		Tape and reel	SN74ALVCHR16269ALR	
	TSSOP – DGG	Tape and reel	SN74ALVCHR16269AGR	ALVCHR16269A
	TVSOP – DGV	Tape and reel	SN74ALVCHR16269AVR	VR269A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES0500–AUGUST 1995–REVISED SEPTEMBER 2004

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to $\overline{OE}$ being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

All outputs are designed to sink up to 12 mA and include equivalent 26- Ω resistors to reduce overshoot and undershoot.

FUNCTION TABLES

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE}A$	$\overline{OE}B$	A	1B, 2B
$\uparrow$	H	H	Z	Z
$\uparrow$	H	L	Z	Active
$\uparrow$	L	H	Active	Z
$\uparrow$	L	L	Active	Active

A-TO-B STORAGE ($\overline{OE}B = L$)

INPUTS			OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B 2B
L	H	$\uparrow$	L	L $2B_0^{(1)}$
L	H	$\uparrow$	H	H $2B_0^{(1)}$
L	L	$\uparrow$	L	L L
L	L	$\uparrow$	H	H H
H	L	$\uparrow$	L	$1B_0^{(1)}$ L
H	L	$\uparrow$	H	$1B_0^{(1)}$ H
H	H	X	X	$1B_0^{(1)}$ $2B_0^{(1)}$

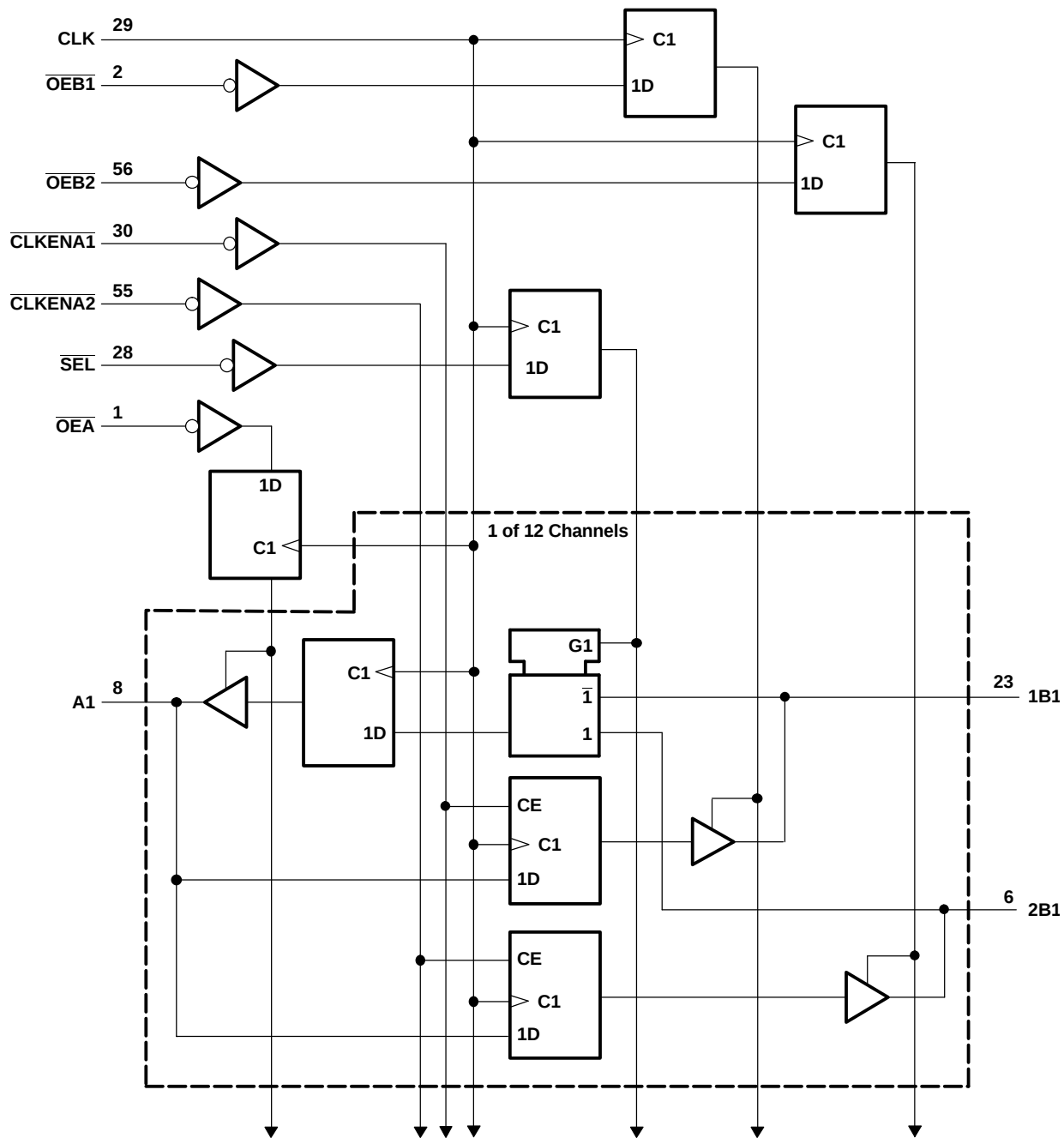
- (1) Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OE}A = L$)

INPUTS				OUTPUT A
CLK	$\overline{SEL}$	1B	2B	
X	H	X	X	$A_0^{(1)}$
X	L	X	X	$A_0^{(1)}$
$\uparrow$	H	L	X	L
$\uparrow$	H	H	X	H
$\uparrow$	L	X	L	L
$\uparrow$	L	X	H	H

- (1) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES0500–AUGUST 1995–REVISED SEPTEMBER 2004

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range	Except I/O ports ⁽²⁾	-0.5	4.6
		I/O ports ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$
V_O	Output voltage range ⁽²⁾⁽³⁾		$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		±50	mA
	Continuous current through each V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	64	°C/W
		DGV package	48	
		DL package	56	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 \text{ V}$	-2	mA
		$V_{CC} = 2.3 \text{ V}$	-6	
		$V_{CC} = 2.7 \text{ V}$	-8	
		$V_{CC} = 3 \text{ V}$	-12	
I_{OL}	Low-level output current	$V_{CC} = 1.65 \text{ V}$	2	mA
		$V_{CC} = 2.3 \text{ V}$	6	
		$V_{CC} = 2.7 \text{ V}$	8	
		$V_{CC} = 3 \text{ V}$	12	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	1.65 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -2 mA	1.65 V	1.2			
	I _{OH} = -4 mA	2.3 V	1.9			
	I _{OH} = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I _{OH} = -8 mA	2.7 V	2			
	I _{OH} = -12 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 2 mA	1.65 V	0.45			
	I _{OL} = 4 mA	2.3 V	0.4			
	I _{OL} = 6 mA	2.3 V	0.55			
		3 V	0.55			
	I _{OL} = 8 mA	2.7 V	0.6			
	I _{OL} = 12 mA	3 V	0.8			
I _I	V _I = V _{CC} or GND	3.6 V			±5	µA
I _{I(hold)}	V _I = 0.58 V	1.65 V	25			µA
	V _I = 1.07 V		-25			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V		-45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V		-75			
	V _I = 0 to 3.6 V ⁽²⁾	3.6 V			±500	
I _{OZ} ⁽³⁾	V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	µA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	5		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	8.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCHR16269A

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES0500–AUGUST 1995–REVISED SEPTEMBER 2004

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	(1)		95		115		135		MHz
t _w	Pulse duration, CLK high or low	(1)		5.2		4.3		3.3		ns
t _{su}	A data before CLK↑	(1)		1.4		1.4		1		ns
	B data before CLK↑	(1)		1.6		1.5		1.1		
	$\overline{\text{SEL}}$ before CLK↑	(1)		0.8		1.1		1.3		
	$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK↑	(1)		0.8		1		0.8		
	$\overline{\text{OE}}$ before CLK↑	(1)		1.7		1.6		1.2		
t _h	A data after CLK↑	(1)		0.9		0.9		1.2		ns
	B data after CLK↑	(1)		0.8		0.6		1		
	$\overline{\text{SEL}}$ after CLK↑	(1)		1.1		0.8		1.7		
	$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK↑	(1)		1.4		1		1.6		
	$\overline{\text{OE}}$ after CLK↑	(1)		0.9		0.8		1.2		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		95		115		135		MHz
t_{pd}	CLK	B	(1)		2.3	7.7	6.9		2.2	5.8	ns
		A	(1)		1.9	6.4	5.8		2	5.2	
t_{en}	CLK	B	(1)		2.5	7.7	6.9		2.3	5.8	ns
		A	(1)		2.2	6.7	6		2.1	5.3	
t_{dis}	CLK	B	(1)		3.3	8.1	6.7		2.4	6	ns
		A	(1)		2.7	8	6.2		2.1	6	

(1) This information was not available at the time of publication.

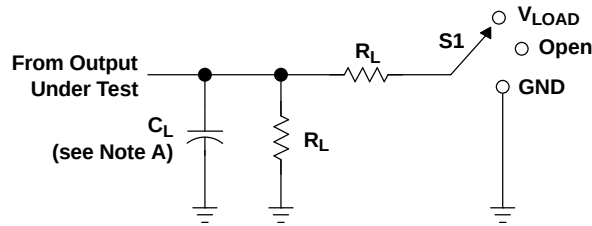
OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Outputs enabled	$C_L = 0, f = 10\text{ MHz}$	(1)	142	172	pF
	Outputs disabled		(1)	115	129	

(1) This information was not available at the time of publication.

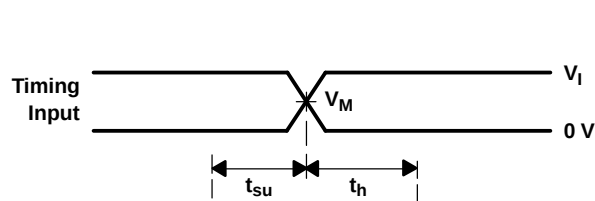
PARAMETER MEASUREMENT INFORMATION



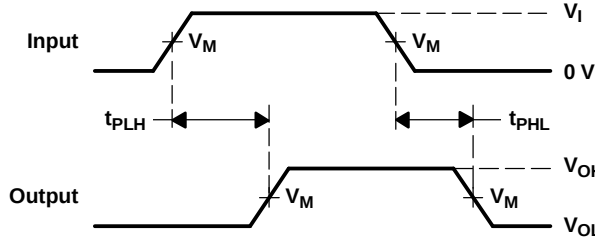
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZH} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

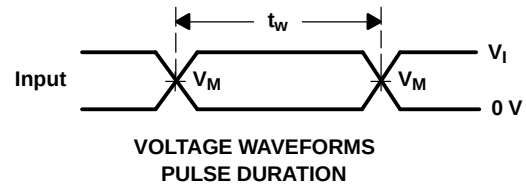
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



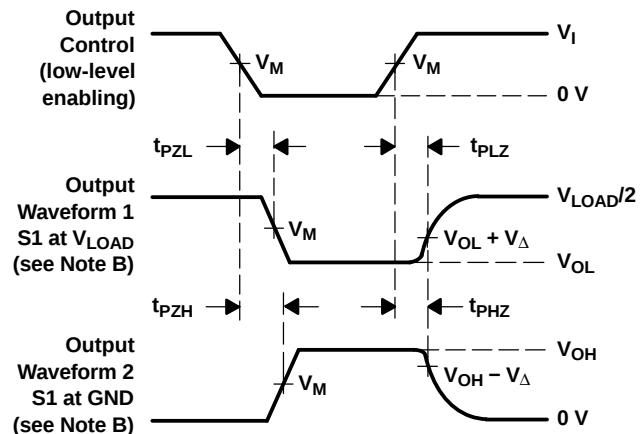
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVCHR16269ALG4	ACTIVE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		Samples
SN74ALVCHR16269AL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

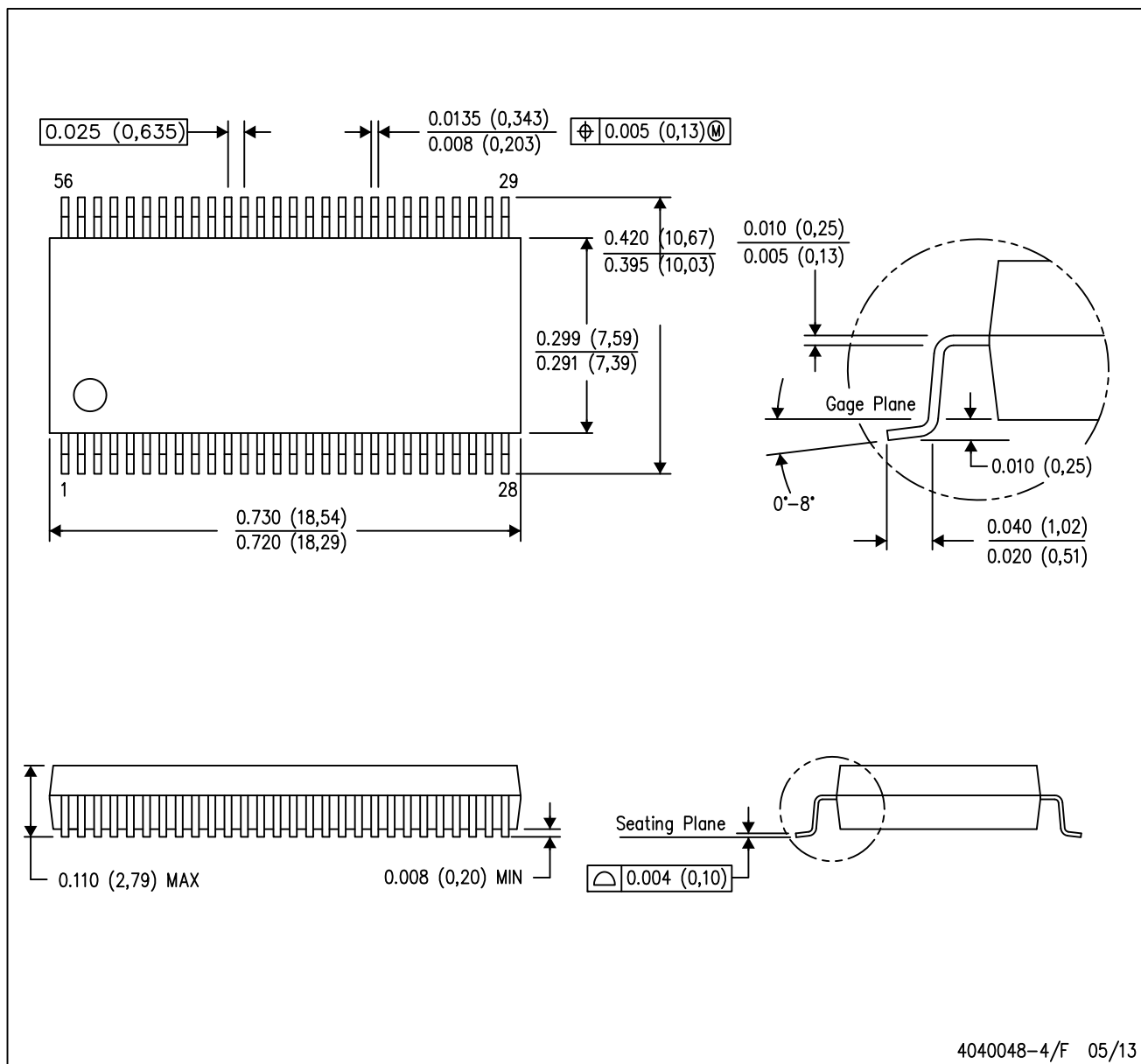
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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